APPENDIX A

The following are marked up versions of the replacement claims indicated in the Reply and Amendment and in accordance with 37 C.F.R. § 1.121. Applicants have used the convention underline to indicate added text and [square brackets] to indicate deleted text.

1. (Once Amended) An optical logic circuit, comprising:

a substrate comprising [of] a first material; [and]

an optical layer overlaying the substrate at least partially comprising a second material, the optical layer configured to provide a plurality of optical pathways, at least one optical pathway configured to transmit an optical bias signal, at least one optical pathway configured to provide an optical input signal, and at least one optical pathway configured to provide an optical output[,] signal; and

an interference region at least partially comprising the second material, configured to selectively cause interference of wavefronts of the optical bias signal and the optical input signal entering the interference region,

wherein the optical output signal is representative of [pathways are configured to provide] a Boolean logic output based on the at least one optical input signal and the optical output signal exits an interference region output.

4. (Once Amended) The optical logic circuit of claim [3] 1, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region [output] when light is provided to the interference region [through the first selective] in the form of the optical input signal.

5. (Once Amended) The optical logic circuit of claim [3] 1, wherein the interference region includes a first selective optical input receiving the optical input signal and a second selective optical input receiving a second optical input signal.

6. (Once Amended) The optical logic circuit of claim 5, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region output when light is provided to the interference region through both the first selective optical input and the second selective optical input.

7. (Once Amended) The optical logic circuit of claim 1, wherein the Boolean logic output is a [representative of the] NOT (inverter) function.

8. (Once Amended) The optical logic circuit of claim 1, wherein the Boolean logic output is a [representative of the] NOT AND (NAND) function.

9. (Once Amended) The optical logic circuit of claim 1, having a multiplicity of optical [logic gates] pathways and interference regions configured to function as an optical processor.

10. (Once Amended) The optical logic circuit of claim 9, wherein the optical processor [is] comprises NOT (inverter) gates and NOT AND (NAND) gates.

11. (Once Amended) An optical logic gate for an optical processor, comprising:

a substrate configured of a first material;

a patterned optical layer overlying the substrate at least partially configured of a second material, the patterned optical layer providing a plurality of optical conduits of the second material, at least [one] two of the optical conduits configured to receive [an] optical input signals, [and] at least one of the optical conduits configured to provide [an] optical output signals, and at least one of the at least two optical input signals being an optical bias input signal; and

an interference region coupled to at least two of the optical conduits configured to receive optical input signals and coupled to at least one of the optical conduits configured to provide optical output signals,

wherein the [optical conduits are] interference region is configured to provide a Boolean logic output signal based on the at least one optical input signal.

13. (Once Amended) The optical logic gate of claim [12] 11, wherein the optical logic gate provides a Boolean NOT function as output.

14. (Once Amended) The optical logic gate of claim 11, further comprising:

at least three optical conduits configured to receive [an] optical [input,] inputs.

[wherein one of the optical inputs is an optical bias input.]

15. (Once Amended) The optical logic gate of claim 14, wherein the optical logic gate provides a Boolean NOT function as output.

21. (Once Amended) The optical logic gate of claim 11, wherein the optical input signal is [optically coupled to] generated by a Laser diode.

22. (Once Amended) The optical logic gate of claim 11, wherein the optical input signal is [optically coupled to] generated by a semiconductor diode.

31. (Once Amended) A method of providing a Boolean logic optical output signal based on at least [one] two optical input signals, comprising:

providing [light] a first selective optical input signal to [the at least one] a first optical input;

providing a plurality of optical pathways formed of optical transmission material patterned on a substrate material;

providing a [light] second selective optical input signal; and

providing at least a portion of the plurality of optical pathways to be configured to selectively cause interference between wavefronts of the first selective optical input signal and the second optical input signal; and

providing an optical output signal, the optical output signal based on the at least [one] two input signals and representative of a Boolean logic function.

36. (Once Amended) An optical logic circuit, comprising:

a substrate comprising a first material; [and]

an optical layer overlaying the substrate at least partially comprising a second material, the optical layer being patterned to provide a plurality of optical pathways, at least [one] two optical [pathway] pathways configured to provide [an] optical input signals, and at least one optical pathway configured to provide an optical output[,] signal; and

an interference region configured to selectively cause interference of wavefronts of light from the optical input signals entering the interference region;

wherein the [optical pathways are] interference region is configured to provide a Boolean logic output signal based on the at least [one] two optical input signals.

38. (Once Amended) The optical logic circuit of claim [37] 36, wherein the interference region includes a first selective input, a bias input, and an interference region output, the bias input transmitting an optical bias signal.

39. (Once Amended) The optical logic circuit of claim 38, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region output when a modulated light signal is provided to the interference region through the first selective input.

41. (Once Amended) The optical logic circuit of claim 40, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region output when light is provided to the interference region through both the first selective input and the second selective input, and when no light is provided to [neither] both of the first and second selective inputs.

42. (Once Amended) The optical logic circuit of claim 36, wherein the Boolean logic output is a [representative of the] NOT (inverter) function.

43. (Once Amended) The optical logic circuit of claim 36, wherein the Boolean logic output is a [representative of the] NOT AND (NAND) function.

44. (Once Amended) The optical logic circuit of claim 36, having a multiplicity of optical [logic gates] pathways and interference regions configured to function as an optical processor.

46. (Once Amended) The optical logic circuit of claim 36, wherein the Boolean logic output is an [representative of the] XOR (exclusive OR) function.